UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,597	11/20/2001	Xiao-Dong Yang	03226.102001;P5991	1542

22511 7590 03/05/2003

ROSENTHAL & OSHA L.L.P.
1221 MCKINNEY AVENUE
SUITE 2800
HOUSTON, TX 77010

EXAMINER
GARBOWSKI, LEIGH M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/989,597	Applicant(s) YANG ET AL.	
	Examin r Leigh Marie Garbowski	Art Unit 2825	

-- Th MAILING DATE of this communication app ars on th cover sh t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. There is insufficient antecedent basis for "the range" in the claim. Thus, the claim is confusing and indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Jones et al. [U.S. Patent #5,629,860].

As per claim 15, Jones et al. disclose a method for creating a wire load model comprising: creating an interconnect configuration [column 1, lines 60-62]; generating parasitic information for the interconnect information, wherein the parasitic information comprises capacitance and resistance information [column 2, lines 23-32]; storing the

parasitic information in an accessible format [column 5, lines 7-12]; and creating the wire load model dependent on the parasitic information [column 5, lines 49-65]. As per claim 16, Jones et al. further disclose wherein generating parasitic information uses an empirical database [column 2, lines 23-32; column 5, lines 49-65], the examiner takes Official Notice that this feature anticipates the use of a field solver. As per claim 17, Jones et al. further disclose wherein creating the wire load model uses a non-linear curve-fitting engine [column 5, lines 52-65]. As per claim 18, Jones et al. further disclose wherein the parasitic information comprises at least once selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance [column 2, lines 23-32].

As per claim 19, Jones et al. disclose a wire load model creation tool comprising: means for creating an interconnect configuration for a structure [column 1, lines 60-62]; means for field solving the interconnect configuration to determine parasitic information, wherein the parasitic information comprises capacitance and resistance information [column 2, lines 23-32; column 5, lines 49-65]; means for storing the parasitic information [column 5, lines 7-12]; curve-fitting means for curve-fitting the parasitic information and using interconnect configuration parameters to create a wire load model [column 5, lines 52-65]; and means for controlling error in the curve-fitting means [column 2, lines 15-22; column 5, line 66-column 8, line 61].

Claims 15-16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yip et al. [U.S. Patent #5,694,344].

As per claim 15, Yip et al. disclose a method for creating a wire load model comprising: creating an interconnect configuration [column 3, lines 60-61]; generating parasitic information for the interconnect configuration, wherein the parasitic information comprises capacitance and resistance information [column 4, lines 58-59]; storing the parasitic information in an accessible format [column 4, lines 21-27]; and creating the wire load model dependent on the parasitic information [column 3, lines 61-64]. As per claim 16, Yip et al. further disclose wherein generating parasitic information uses a field solver [column 4, lines 58-63]. As per claim 18, Yip et al. further disclose wherein the parasitic information comprises at least once selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance [column 2, lines 31-35].

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ponnapalli et al. [U.S. Patent #6,175,947].

As per claim 1, Ponnapalli et al. disclose a method for creating a wire load model comprising: creating an interconnect configuration [column 5, lines 16-28]; running a field solver to generate parasitic information for the interconnect information [column 2, lines 30-34; column 7, lines 13-15]; storing the parasitic information in an accessible format, wherein the parasitic information comprises capacitance and resistance information [column 6, lines 26-31; column 7, line 15]; and running a curve fitting engine to create the wire load model, wherein running the curve-fitting engine is dependent on the parasitic information [column 8, lines 19-28]. As per claim 2, Ponnapalli et al. further disclose wherein a range of widths and spacings for the interconnect configuration are

chosen so that widths and spacings are larger than a minimum width and spacing specification for the interconnect configuration [column 7, lines 54-64; column 8, lines 20-28]. As per claim 3, Ponnapalli et al. further disclose wherein the accessible format is a look-up table [column 12, lines 42, 58]. As per claim 4, Ponnapalli et al. further disclose wherein the curve-fitting engine is non-linear [column 7, lines 61-62; column 8, line 27]. As per claim 5, Ponnapalli et al. further disclose wherein the parasitic information comprises at least once selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance [figures 8-9]. As per claim 20, Ponnapalli et al. further disclose wherein the interconnect configuration is non-symmetrical [column 8, lines 20-22].

As per claims 6-18, Ponnapalli et al. disclose the similar method as outlined above with respect to claims 1-5, including the use of a program storage device and computer system [column 10, line 44].

As per claim 19, Ponnapalli et al. disclose a tool for creating a wire load model comprising: means for creating an interconnect configuration for a structure [column 5, lines 16-28]; means for field solving the interconnect configuration to determine parasitic information, wherein the parasitic information comprises capacitance and resistance information [column 2, lines 30-34; column 7, lines 13-15]; means for storing the parasitic information [column 6, lines 26-31; column 7, line 15]; means for curve-fitting the parasitic information and using interconnect configuration parameters to create a wire load model [column 8, lines 19-28]; and means for controlling error in the curve-fitting means [column 12, lines 4-6].

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chou et al. [U.S. Patent #6,291,254 B1].

As per claim 1, Chou et al. disclose a method for creating a wire load model comprising: creating an interconnect configuration [column 8, lines 49-50]; running a field solver to generate parasitic information for the interconnect information [column 1, lines 34-39; column 8, lines 51-52]; storing the parasitic information in an accessible format, wherein the parasitic information comprises capacitance and resistance information [column 9, lines 18-44]; and running a curve fitting engine to create the wire load model, wherein running the curve-fitting engine is dependent on the parasitic information [column 9, lines 14-16; column 10, lines 33-37]. As per claim 2, Chou et al. further disclose wherein a range of widths and spacings for the interconnect configuration are chosen so that widths and spacings are larger than a minimum width and spacing specification for the interconnect configuration [column 13, lines 35-40]. As per claim 3, Chou et al. further disclose wherein the accessible format is a look-up table [Table 1]. As per claim 4, Chou et al. further disclose wherein the curve-fitting engine is non-linear [column 9, lines 14-16]. As per claim 5, Chou et al. further disclose wherein the parasitic information comprises at least once selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance [column 1, lines 28-39]. As per claim 20, Chou et al. further disclose wherein the interconnect configuration is non-symmetrical [column 8, lines 27-43].

As per claims 6-18, Chou et al. disclose the similar method as outlined above with respect to claims 1-5, including the use of a program storage device and computer system [figure 3; column 1, line 34].

As per claim 19, Chou et al. disclose a tool for creating a wire load model comprising: means for creating an interconnect configuration for a structure [column 8, lines 49-50]; means for field solving the interconnect information to determine parasitic information, wherein the parasitic information comprises capacitance and resistance information [column 1, lines 34-39; column 8, lines 51-52]; means for storing the parasitic information [column 9, lines 18-44]; means for curve-fitting the parasitic information and using interconnect configuration parameters to create a wire load model [column 9, lines 14-16; column 10, lines 33-37]; and means for controlling error in the curve fitting means [column 9, lines 2-3].

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chang et al. [U.S. Patent #6,381,730 B1] disclose creating wireload models using parasitic extraction involving field solving and curve fitting. Graef et al. [U.S. Patent #6,189,131 B1] disclose creating wireload models in a range of values.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 703-305-9753. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communication and 703-872-9319 After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

Leigh Marie Garbowski
February 26, 2003

LEIGH M. GARBOWSKI
PATENT EXAMINER